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Application of eLOCOS™ EMP Technology to Improve Electrical and Thermal Conductivity of LTCC Interconnects

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Vision: Nano3D Systems eLOCOS™ EMP technology can be implemented with low temperature co-fired ceramics (LTCC) to increase power density by providing better electrical and thermal conductivity for interconnects.

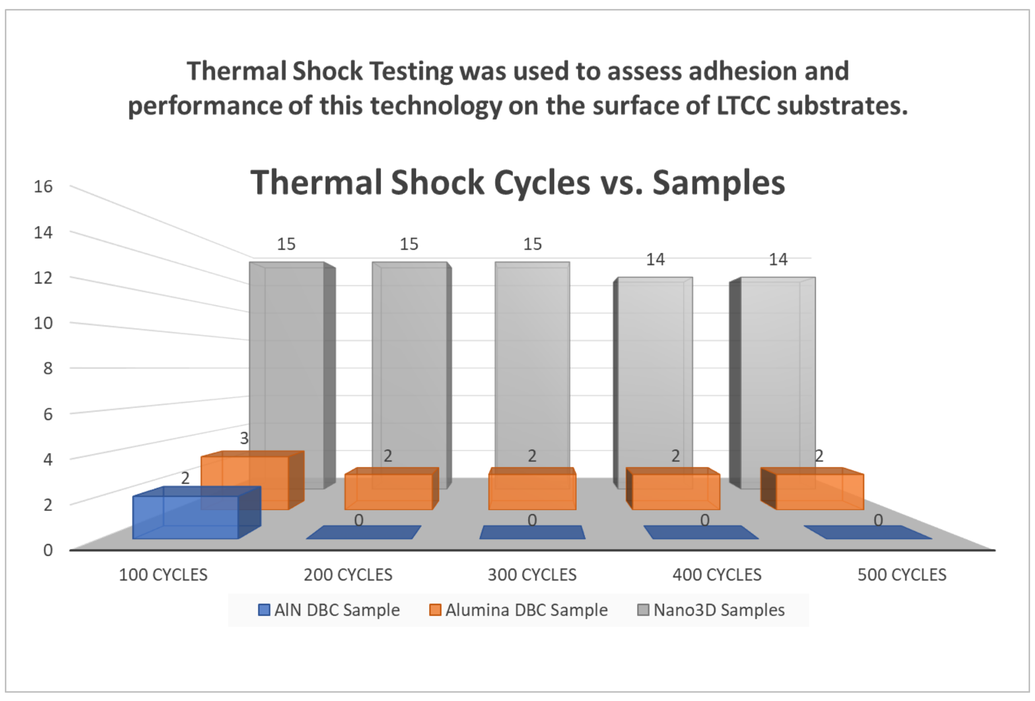
- Nano3D Systems eLOCOS™ metallization platform technology for high density interconnects
  - Electrochemical
  - Low cost
  - Selective and Scalable
- Nano3D Systems uses an electroless metal photo-patterning (EMP) technology
  - Minimizing cost and waste

Thermal Conductivity (W/m*K)	
DuPont™ 6141 Silver Via Fill [1]	Copper
289	401

[1] M. A. Zampino, R. Kandukuri and W. K. Jones, "High performance thermal vias in LTCC substrates," ITherm 2002, pp. 179-185.

Electrical Resistivity (mΩ/sq.)	
LTCC Thick Film Paste DuPont™ 6142D Ag	1 oz. Copper Sheet
3.3	0.5

Key Results



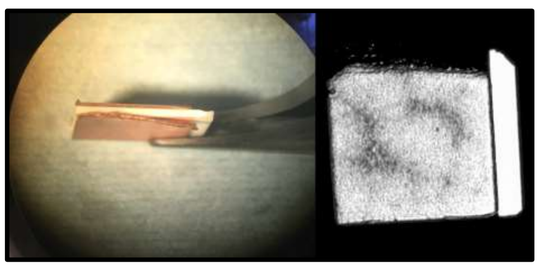


Fig. 1 (left) Alumina DBC Samples after 200 cycles of thermal shock. Left: Microscope Image; Right: SAM Image

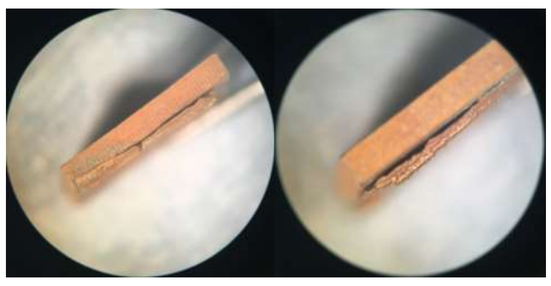


Fig. 2 One sample showed obvious delamination after 400 thermal shock cycles

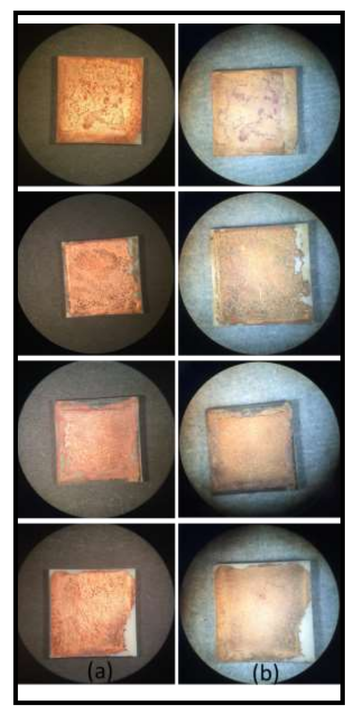


Fig. 3. (left) Surface variations of the Cu but no obvious delamination. Samples shown (a) before thermal shock testing (b) after 500 thermal shock cycles.

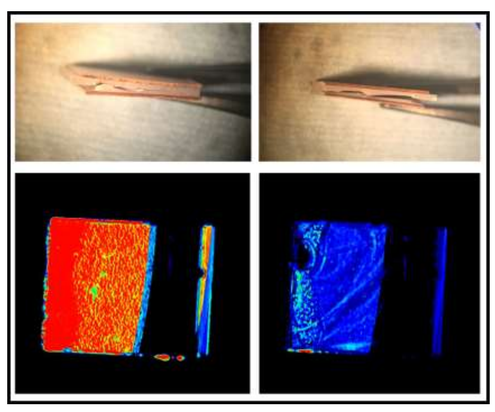


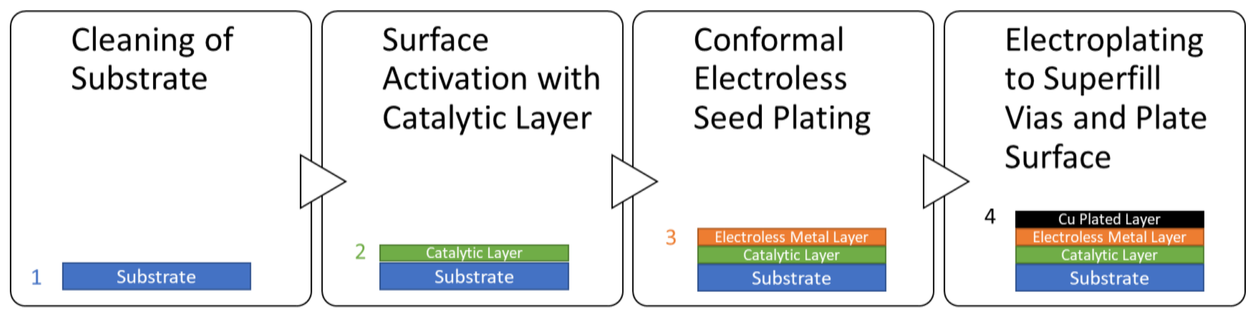
Fig. 4 AlN DBC Samples after 200 cycles of thermal shock. Top: Microscope Images of cracked ceramic; Bottom: SAM Images of one of the samples

Methodology and Approaches

Thermal Shock Testing Conditions	
Temperature Range (°C) (JESD22-A106B)	-55 - 125
Shock Dwell Time (MIL-STD-202G)	5 minutes
Ambient Temperature Dwell Time (JESD22-A106B)	< 20 seconds

Fig. 5 Thermal Shock Testing Set Up (a) Test Fixture (b) Inside Thermal Shock Chamber

Plating Process Flow



Future Work

- Investigate the effects of thermal shock on Cu filled through hole vias in LTCC substrates.
- Design power module that utilizes this technology and compare to conventional LTCC fabrication processes.

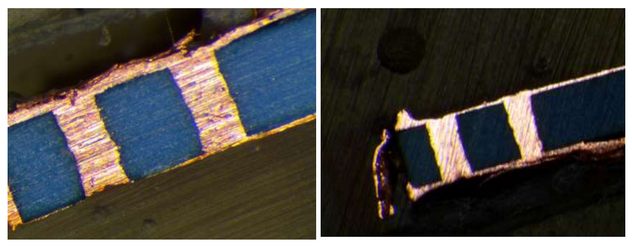


Fig. 6 Cross section of 20 mil vias filled with optimized plating conditions to minimize overburden plating.

P/O/E/T/S